Claims

1. A semiconductor device including a dual damascene structure formed in a dielectric stack, the stack comprising an upper layer having a first formation etched therein, an intermediate etch stop layer and a lower layer having a second formation etched therein, the second formation being contiguous with the first through the etch stop layer, each of the layers having a dielectric constant $k \leq 3.5$ and the etch stop layer has a selectivity of at least 2.5:1 relative to the upper layer.

2. A device as claimed in Claim 1 wherein the etch stop layer is integral with the lower layer.

3. A device as claimed in Claim 1 or Claim 2 wherein the etch stop layer is formed of nitrogen-doped silicon carbide.

4. A method of forming a low k film on a substrate comprising:

(a) positioning the substrate on a support in a chamber.

(b) supplying to the chamber in gaseous or vapour from a silicon-containing organic compound and nitrogen in the presence of a plasma to deposit a nitrogen-doped silicon carbide film on the substrate.

5. A method as claimed in Claim 5 where the nitrogen-doped silicon carbide is deposited by a plasma driven at frequencies below 4 mHz.

6. A method as claimed in Claim 4 or Claim 5 wherein the silicon-containing organic compound is an alkylsilane.

7. A method as claimed in any one of Claims 4 to 6 wherein the silicon-containing compound is a tetraalkysilane.

8. A method as claimed in any one of Claims 4 to 6 wherein the silicon-containing organic compound is tetramethylsilane.

9. An etch stop layer comprising nitrogen doped silicon carbide.

10. A stack of dielectric layers when in each layer is formed of a different material, the materials having detectably different etch characteristics but generally equal dielectric constants.

11. A stack as claimed in Claim 10 wherein the selectivity between adjacent layers is at least 2.5:1.

12. A method of forming a dual damascene structure including depositing a layer of first insulating material having a first etch rate on a semiconductor wafer, part etching one or more vias in the first layer, subsequentially depositing a layer of second insulating material onto the first so that the part etched via is filled with the second material causing a corresponding formation to appear at the surface of the second layer,

etching the second layer a channel to receive a wiring line such that the channel contains the corresponding formation, the relative etch rates of the materials being such that when the channel is etched to the surface of the first layer, the via is fully etched through the first layer.

13. A stack as claimed in Claim 10 or Claim 11 wherein the difference in the dielectric constants of the materials of adjacent layers varies by less than 10%

14. A method as claimed in Claim 13 wherein the etch rate of the first layer is approximately twice that of the second layer.

15. A method as claimed in Claim 12 wherein the first layer is carbon-doped SiO_2 and the second layer is nitrogen-doped SiC or carbon-doped silicon nitride.

16. A method of forming a low k etch stop layer comprising depositing carbon-doped SiO_2 by a plasma based reaction at a frequency below 4 mHz and depositing a nitrogen-doped SiC by a plasma based reaction onto the SiO_2 material at a frequency below 4 mHz.